IN THE CLAIMS

1. (Original) A content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, each array group having a group global mask for storing a mask pattern indicating priority of the array group.

2. (Original) The CAM system of Claim 1, wherein two or more array groups have the same priority.

3. (Original) The CAM system of Claim 1, wherein the priority comprises a prefix of a classless inter-domain routing (CIDR) address.

4. (Original) The CAM system of Claim 3, further comprising:

means for generating an index of the longest prefix match in response to a comparison between a search key and data stored in the array groups.

5. (Original) The CAM system of Claim 3, further comprising:

means for storing data in the array groups according to prefix.

6. (Original) The CAM system of Claim 1, further comprising:

means for selectively comparing a search key with data stored in the array groups according to priority.

7. (Original) The CAM system of Claim 6, wherein the means for selectively comparing comprises:

means for receiving a priority for the search key; and

means for comparing the search key with data stored only in the array groups that have the same priority as the search key.

8. (Original) The CAM system of Claim 6, wherein the means for selectively comparing comprises:

means for comparing the search key with data stored in the array groups;

means for comparing a priority of the search key with the priority of each array group; and

means for selectively enabling results of the comparison of the search key and the data in each array group in response to the comparison of their priorities.

9. (Original) The CAM system of Claim 8, wherein the means for comparing the priorities includes a priority table for storing the priority of each array group.

10. (Currently Amended) The CAM system of Claim 6, wherein the means for selectively comparing comprises:

a select circuit having a plurality of inputs to receive match signals from the plurality of array groups during a compare operation between ~~a~~ the search key and data stored in the array groups, and having a plurality of outputs to provide qualified match signals for the plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified match signals, and having an output to generate an index of the highest priority match in response to the qualified match signals.

11. (Original) The CAM system of Claim 10, wherein the select circuit includes means for selectively forcing the qualified match signals to a mismatch state according to priority.

12. (Original) The CAM system of Claim 10, wherein the select circuit passes only the match signals from array groups having the same priority as the search key, while disqualifying the match signals from other array groups.

13. (Original) The CAM system of Claim 10, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the match signals from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the match signals to the priority encoder as qualified

match signals in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the search key and the priorities of the array groups.

14. (Original) The CAM system of Claim 13, wherein the compare circuit further comprises a priority table having a plurality of rows, each for storing the priority of a corresponding array group.

15. (Original) The CAM system of Claim 14, wherein the select circuit further comprises a plurality of group match flag circuits, each receiving the match signals from a corresponding array group and generating a group match flag in response thereto, wherein the group match flags are provided as select signals to corresponding rows of the priority table.

16. (Original) The CAM system of Claim 1, further comprising:

means for storing data in the array groups according to priority.

17. (Original) The CAM system of Claim 16, wherein the means for storing comprises an address circuit having a first input to receive the priority of the data, a second input to receive a next free address (NFA) corresponding to the priority, and having outputs coupled to the array groups.

18. (Original) The CAM system of Claim 17, wherein the address circuit comprises an address decoder to select a row in one array group corresponding to the priority in response to the NFA.

19. (Original) The CAM system of Claim 18, wherein the address circuit further comprises an NFA table having a number of rows, each row for storing the NFA for a corresponding priority.

20. (Original) The CAM system of Claim 19, wherein each row in the NFA table includes an empty bit indicative of whether any array group is assigned to the corresponding

priority.

21. (Original) The CAM system of Claim 16, wherein the means for storing data comprises an index circuit to generate a next free address (NFA) for the data according to its priority.

22. (Original) The CAM system of Claim 21, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive valid bits from the plurality of array groups, the valid bits indicating whether valid data is stored in corresponding rows of the array group, and having a plurality of outputs to provide qualified valid bits for the plurality of array groups; and

a priority encoder having a plurality of inputs to receive the plurality of qualified valid bits, and having an output to generate the NFA in response to the qualified valid bits.

23. (Original) The CAM system of Claim 22, wherein the select circuit includes means for selectively forcing the qualified valid bits to a mismatch state according to priority.

24. (Original) The CAM system of Claim 22, wherein the select circuit passes only the valid bits from array groups having the same priority as the data, while disqualifying the valid bits from other array groups.

25. (Original) The CAM system of Claim 22, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the valid bits from a corresponding array group, a second input to receive an enable signal for the corresponding array group, and outputs to selectively provide the valid bits to the priority encoder as qualified valid bits in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the data and the priorities of the array groups.

26. (Original) The CAM system of Claim 25, wherein the compare circuit further comprises:

an input to receive the priority of the data; and

a table having a plurality of rows, each for storing the priority of a corresponding array group.

27. (Original) The CAM system of Claim 22, wherein the index circuit further comprises:

a group priority encoder having a plurality of inputs to receive a mask valid bit from each of the plurality of array groups, the mask valid bits indicating whether valid mask patterns are stored in corresponding group global masks of the array groups, and having an output to generate a first portion of the NFA for the data.

28. (Original) The CAM system of Claim 27, wherein the index circuit further comprises a full flag circuit for generating a full flag in response to the qualified valid bits to indicate whether there are any available rows in array groups having the same priority as the data.

~~30~~ 29. (Currently Amended) A content addressable memory (CAM) system, comprising:

an array of binary CAM cells segmented into a plurality of array groups, each array group assigned a priority; and

a priority table including a plurality of rows, each for storing the priority of a corresponding array group.

30. (Original) The CAM system of Claim 29, wherein two or more array groups are assigned the same priority.

31. (Original) The CAM system of Claim 29, wherein each array group includes a group global register for storing a global mask pattern indicative of the priority of the array group.

32. (Original) The CAM system of Claim 29, further comprising:

means for selectively comparing a search key with data stored in the array groups according to priority to generate a highest-priority match (HPM) index.

33. (Original) The CAM system of Claim 32, wherein the means for selectively comparing comprises:

means for comparing the search key with data stored in each array group to generate match signals;

means for comparing a priority of the search key with the priority of each array group to generate enable signals; and

means for selectively allowing the match signals to participate in the generation of the HPM index in response to the enable signals.

34. (Original) The CAM system of Claim 33, wherein the means for selectively allowing forces to a mismatch state the match signals of one or more array groups whose priority does not match the priority of the search key.

35. (Original) The CAM system of Claim 33, wherein the means for selectively allowing allows the match signals of one or more array groups whose priority best matches the priority of the search key to participate in the generation of the HPM index.

36. (Currently Amended) The CAM system of Claim 29, further comprising:

~~means for comparing a search key with data storing the array groups according to priority~~ means for storing data in the array groups according to priority.

37. (Original) The CAM system of Claim 36, wherein the means for storing comprises:

means for generating a next free address (NFA) for each of a number of priorities;

an input to receive a priority for the data;

an NFA table having a number of rows, each for storing the NFA for a corresponding priority, the NFA table outputting the NFA indicated by the priority of the data; and

an address decoder for selecting a row in the array in response to the NFA provided by the NFA table.

38. (Original) The CAM system of Claim 37, wherein each row in the NFA table includes an empty bit indicative of whether any array group is assigned to the corresponding priority.

39. (Currently Amended) A method of operating a content addressable memory (CAM) system including an array of binary CAM cells segmented into a plurality of array groups, comprising:

assigning a priority to one or more array groups; and

selectively storing data in the array groups according to priority, wherein assigning the priority comprises:

for each array group, storing a mask pattern indicative of the priority assigned to the array group in a global mask for the array group.

40. (Original) The method of Claim 39, wherein two or more array groups are assigned the same priority.

41. (Canceled)

42. (Original) The method of Claim 39, wherein the selectively storing data comprises:

receiving a priority of the data;

providing a next free address (NFA) corresponding to one of the array groups assigned to the priority of the data; and

storing the data in the array at the NFA.

43. (Currently Amended) The method of Claim ~~39~~ 42, wherein providing the NFA comprises:

generating an NFA for each priority;

storing the NFA for each priority in a corresponding row of an NFA table;

selecting a row of the NFA table using the priority of the data; and

accessing the NFA corresponding to the priority of the data.

44. (Original) The method of Claim 43, wherein generating the NFA comprises:

providing valid bits from each array group, the valid bits indicating whether valid data is stored in corresponding rows of each array group;

for each array group, comparing the priority of the data with the priority of the array group to generate an enable signal;

selectively allowing, in response to the enable signals, the valid bits from corresponding array groups to participate in the generation of the NFA.

45. (Original) The method of Claim 44, wherein the selectively allowing comprises:

selectively qualifying the valid bits from each array group in response to the corresponding enable signal to generate qualified valid bits; and

generating the NFA in response to the qualified valid bits.

46. (Original) The method of Claim 45, wherein selectively qualifying comprises:

forcing to a mismatch state the valid bits from each array group whose priority does not match the priority of the search key.

47. (Original) The method of Claim 45, wherein selectively qualifying comprises:

allowing the valid bits from each array group whose priority matches the priority of the search key to participate in the generation of the NFA.

48. (Original) The method of Claim 43, wherein generating the NFA further comprises:

for each array group, storing a mask valid bit indicative of whether the array group is

assigned to one of the priorities; and

generating a first portion of the NFA in response to the mask valid bits, the first portion of the NFA identifying one of the array groups that is not assigned to one of the priorities.

49. (Original) The method of Claim 39, wherein the priority comprises a prefix of a classless inter-domain routing (CIDR) address.

50. (Original) The method of Claim 49, further comprising:

generating an index of the longest prefix match in response to a comparison between a search key and data stored in the array groups.

51. (Original) The method of Claim 39, further comprising:

selectively comparing a search key with data stored in the array groups according to priority.

52. (Original) The method of Claim 51, wherein the selectively comparing comprises:

comparing the search key with data stored in the array groups to generate match signals;

for each array group, comparing a priority of the search key with the priority of the array group to generate an enable signal; and

for each array group, selectively qualifying the match signals in response to the enable signal to generate qualified match signals.

53. (Original) The method of Claim 52, wherein the selectively qualifying comprises:

forcing to a mismatch state the match signals for each array group whose priority does not match the priority of the search key.

54. (Original) The method of Claim 52, wherein the selectively qualifying comprises:

enabling the match signals for each array group whose priority best matches the priority

of the search key.

55. (Original) The method of Claim 52, further comprising:

generating an index of the highest priority match (HPM) in response to the qualified match signals.

56. (Original) The method of Claim 55, wherein the selectively qualifying comprises:

allowing the match signals from each array group whose priority best matches the priority of the search key to participate in the generation of the HPM index.

57. (Original) The method of Claim 39, further comprising storing the priority for each array group in a priority table.

58. (New) The CAM system of Claim 1, further comprising:

a plurality of mask valid bits, each mask valid bit indicating whether a corresponding group global mask stores a valid mask pattern.

59. (New) The CAM system of Claim 31, further comprising:

a plurality of mask valid bits, each mask valid bit indicating whether a corresponding group global register stores a valid mask pattern.

60. (New) A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells; and

a plurality of group global mask circuits each coupled to a corresponding one of the CAM array groups and each for storing a group global mask for globally masking one or more bits in all of the rows of CAM cells of the corresponding CAM array group, wherein each group global mask indicates a priority of the corresponding group of CAM cells relative to other CAM array groups.

61. (New) The CAM of Claim 60, wherein the priority assigned to each CAM array

group is unrelated to the CAM array group's location relative to other CAM array groups.

62. (New) The CAM of Claim 60, wherein each row of binary CAM cells further comprises a valid bit indicating whether valid data is stored in the row.

63. (New) The CAM of Claim 60, further comprising a plurality of mask valid bits, each indicating whether a valid global mask is stored in a corresponding group global mask circuit.

64. (New) The CAM of Claim 63, wherein each mask valid bit indicates whether a corresponding CAM array group is assigned to a CIDR prefix.

65. (New) The CAM of Claim 60, further comprising:

an index circuit for generating an index of the highest priority match, the index circuit responsive to match information corresponding to the rows of binary CAM cells and to mask information corresponding to the CAM array groups.

66. (New) The CAM of Claim 65, wherein the index circuit further comprises:

a select circuit having first inputs to receive match signals from corresponding rows of binary CAM cells, having second inputs to receive the mask information from corresponding group global mask circuits, and having outputs to provide qualified match signals; and

a priority encoder having inputs to receive the qualified match signals, and having an output to generate the index of the highest priority match in response to the qualified match signals.

67. (New) The CAM of Claim 66, wherein the select circuit comprises:

a plurality of match flag circuits, each having inputs to receive the match signals from a corresponding CAM array group, and having an output to generate a group match flag;

a compare circuit having first inputs to receive the group match flags, and configured to compare only the group global masks corresponding to the CAM array groups that have an

asserted group match flag to generate enable signals indicative of which of the CAM array groups have the highest priority; and

a plurality of enable circuits, each having first inputs to receive the match signals from a corresponding CAM array group, a second input to receive a corresponding enable signal, and a plurality of outputs to generate the qualified match signals.

68. (New) The CAM of Claim 67, wherein the select circuit further comprises:

a priority table having a plurality of rows, each for storing the priority of a corresponding CAM array group.

69. (New) The CAM of Claim 60, further comprising:

an index circuit for generating a next free address (NFA) for data to be stored in the CAM, the NFA indicating an available row in a CAM array group that has the priority as the data.

70. (New) The CAM of Claim 69, wherein the index circuit comprises:

a select circuit having first inputs to receive a valid bit from corresponding rows of binary CAM cells, a second input to receive the priority of the data, and outputs to generate a plurality of qualified valid bits; and

an array priority encoder having inputs to receive the qualified valid bits, and having an output to generate a first portion of the NFA in response to the qualified valid bits, the first portion of the NFA identifying a particular row.

71. (New) The CAM of Claim 70, wherein the index circuit further comprises:

a group priority encoder having inputs to receive a mask valid bit from each CAM array group, the mask valid bits indicating whether corresponding CAM array groups are assigned a priority, and having an output to generate a second portion of the NFA in response to the mask valid bits, the second portion of the NFA identifying a particular CAM array group.

72. (New) The CAM of Claim 71, wherein the index circuit further comprises:

an NFA table having a plurality of rows each for storing the NFA for a corresponding priority, the NFA table including inputs coupled to the array priority encoder and to the group priority encoder.

73. (New) A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells; and

means for assigning a first priority to a first and a second of the CAM array groups, and for assigning a second priority to a third of the CAM array groups, wherein the first and second priorities are different, and wherein the third CAM array group occupies an address space numerically between address spaces occupied by the first and second CAM array groups.

74. (New) The CAM system of Claim 73, further comprising:

means for storing data in the CAM array groups according to priority.

75. (New) The CAM system of Claim 74, wherein the means for storing comprises an address circuit having a first input to receive the priority of the data, a second input to receive a next free address (NFA) corresponding to the priority, and having outputs coupled to the CAM array groups.

76. (New) The CAM system of Claim 75, wherein the address circuit comprises an address decoder to select a row in one CAM array group corresponding to the priority in response to the NFA.

77. (New) The CAM system of Claim 76, wherein the address circuit further comprises an NFA table having a number of rows, each row for storing the NFA for a corresponding priority.

78. (New) The CAM system of Claim 77, wherein each row in the NFA table includes an empty bit indicative of whether any CAM array group is assigned to the corresponding priority.

79. (New) The CAM system of Claim 74, wherein the means for storing data comprises an index circuit to generate a next free address (NFA) for the data according to its priority.

80. (New) The CAM system of Claim 79, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive valid bits from the plurality of CAM array groups, the valid bits indicating whether valid data is stored in corresponding rows of each CAM array group, and having a plurality of outputs to provide qualified valid bits for the plurality of CAM array groups; and

a priority encoder having a plurality of inputs to receive the qualified valid bits, and having an output to generate the NFA in response to the qualified valid bits.

81. (New) The CAM system of Claim 80, wherein the select circuit includes means for selectively forcing the qualified valid bits to a mismatch state according to priority.

82. (New) The CAM system of Claim 80, wherein the select circuit passes only the valid bits from CAM array groups having the same priority as the data, while disqualifying the valid bits from other CAM array groups.

83. (New) The CAM system of Claim 80, wherein the select circuit further comprises:

a plurality of logic gates, each having first inputs to receive the valid bits from a corresponding CAM array group, a second input to receive an enable signal for the corresponding CAM array group, and outputs to selectively provide the valid bits to the priority encoder as qualified valid bits in response to the enable signal; and

a compare circuit for generating the enable signals in response to a comparison between the priority of the data and the priorities of the CAM array groups.

84. (New) The CAM system of Claim 83, wherein the compare circuit further comprises:

an input to receive the priority of the data; and

a table having a plurality of rows, each for storing the priority of a corresponding CAM array group.

85. (New) A content addressable memory (CAM) comprising:

a plurality of CAM array groups each including a plurality of rows of binary CAM cells each coupled to a corresponding match line;

a plurality of group global mask circuits each coupled to a corresponding one of the array groups and each for storing a group global mask for globally masking one or more bits in all of the rows of binary CAM cells of the corresponding array group; and

an index circuit coupled to the match lines to determine, as between rows of CAM cells in different array groups that contain data matching a search key as masked by their corresponding group global masks, an index of one of the rows of CAM cells that contains the data matching the search key, wherein one of the rows of CAM cells has a corresponding group global mask that masks fewer bits than the other group global masks associated with the other rows of CAM cells that store data matching the search key.

86. (New) The CAM system of Claim 85, wherein the index circuit comprises:

a select circuit having a plurality of inputs to receive match signals on the match lines, and having a plurality of outputs to provide qualified match signals; and

a priority encoder having a plurality of inputs coupled to the outputs of the select circuit to receive the plurality of qualified match signals, and having an output to provide the index of the one of the rows of CAM cells that contains the data matching the search key.

87. (New) The CAM system of Claim 86, wherein the select circuit further comprises:

a plurality of match circuits each having inputs coupled to receive the match signals from match lines of a corresponding one of the array groups, and each having an output to provide a group match flag signal indicative of whether one the match signals indicates a match between the search key and data stored in at least one of the rows of CAM cells of the corresponding array group;

a compare circuit having inputs to receive the group match flag signals and adapted to compare the group global masks associated with only the array groups having a group match flag signal set to a match state, the compare circuit having outputs to provide enable signals indicative of which of the group global masks are adapted to mask the most bits; and

enable logic coupled to the outputs of the compare circuit to receive the enable signals and further coupled to the match lines to receive the match signals, wherein the enable signals selectively qualify the match signals.

88. (New) The CAM of Claim 87, wherein the compare circuit further comprises a priority table having a plurality of rows, each for storing the priority of a corresponding array group.